

Figure 1

```
graph TD; Processor[Processor 238] <--> IOPorts[I/O Data Ports 246]; Processor <--> Display[Display 234]; Processor <--> Memory[Memory 236]; Processor <--> Input[Input Devices 232]; Processor <--> Speaker[Speaker 244]; Processor <--> Storage[Storage System 242];
```

Data Processing System  
230

Figure 2

Figure 3

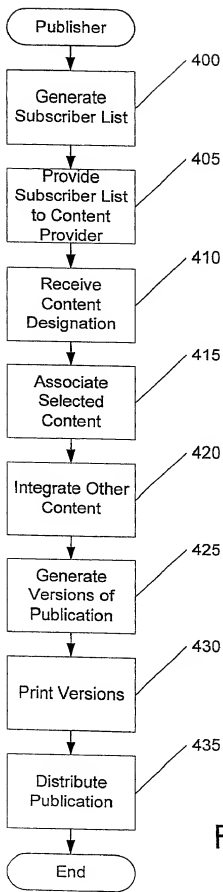


Figure 4

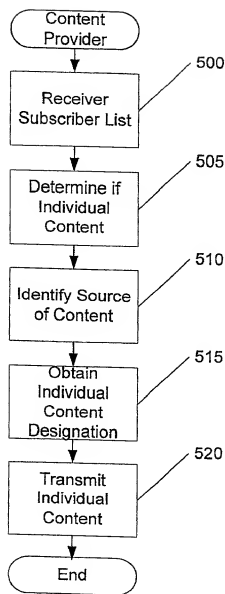


Figure 5